RapidSmith – Rapid Prototyping FPGA Design Tools

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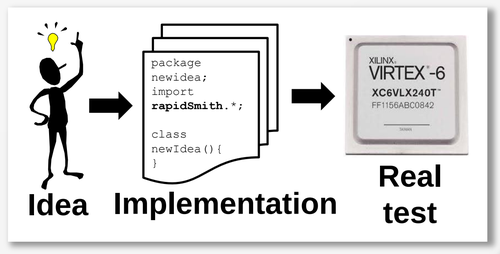
What is RapidSmith?

SUMMARY
- RapidSmith is a research-based FPGA CAD tool written in Java for modern Xilinx FPGAs
- Based on XDL, its objective is to serve as a rapid prototyping platform for research ideas and algorithms relating to low level FPGA CAD tools

DEVICE AND TOOL SUPPORT
- Currently RapidSmith supports the Xilinx FPGAs in the Virtex 4, Virtex 5 and Virtex 6 families
- It aims to be fully compatible with all modern Xilinx FPGAs
- RapidSmith works with Xilinx ISE 11.1 and above

GOALS
- To provide an easy-to-use rapid prototyping platform for new FPGA CAD algorithms and ideas
- Provide useful infrastructure to demonstrate new and unique ideas on real Xilinx FPGAs



CHECK OUT RAPIDSMITH AT:
http://rapidsmith.sourceforge.net

Java

*RapidSmith requires some Xilinx tools for installation which only run on Windows or Linux

GPL

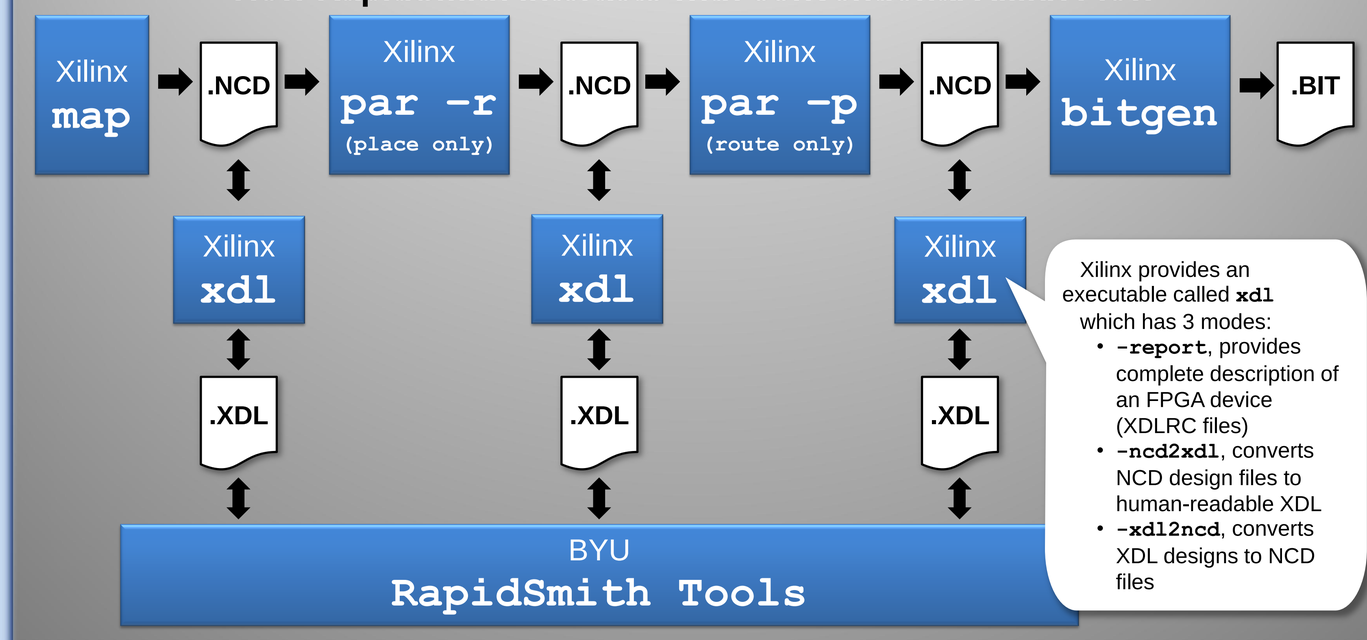
What is XDL?

SUMMARY
- Xilinx has a human-readable native netlist equivalent to NCD called XDL
- This provides RapidSmith a gateway to create tools and manipulate Xilinx designs at a very low level

XDL DEVICE REPORTS (XDLRC FILES)
- Describes an entire FPGA and its resources
- Represents device as a 2D array of "Tiles"
  - Each tile has primitive sites, wires and PIPs
  - Enough information to build entire tool chains
- These files are very large (several gigabytes)

XDL DESIGNS
- XDL describes designs at the FPGA primitive level (SLICES, DSP, …)
- XDL can represent designs that are:
  - unplaced and unrouted
  - partially or fully placed and unrouted
- fully placed and partially or fully routed
- XDL design files have 2 common statements:
  - **`instance`**
    - An FPGA primitive instance in the design with configuration and placement information
  - **`net`**
    - Details pins, sources and sinks and how they are connecting in the routing resources

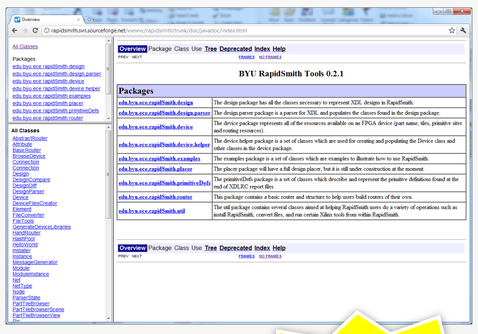
How RapidSmith interacts with conventional Xilinx Flow



Xilinx provides an executable called **`xdl`** which has 3 modes:
- **`-report`**, provides complete description of an FPGA device (XDLRC files)
- **`-ncd2xdl`**, converts NCD design files to human-readable XDL
- **`-xdl2ncd`**, converts XDL designs to NCD files

What's in RapidSmith?

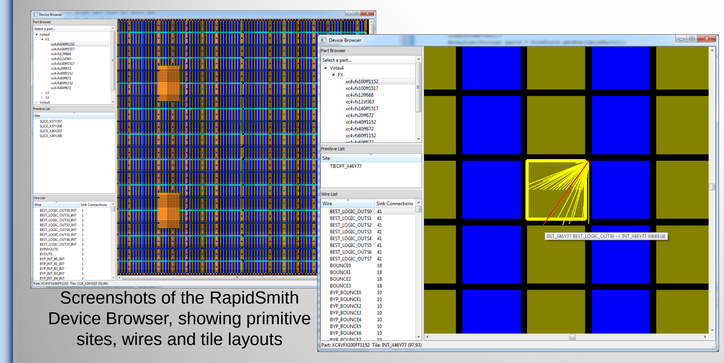
OVERVIEW
- 70+ classes, over 650 APIs in RapidSmith
- 225 APIs in the `design` package alone for manipulating designs in RapidSmith
- Package names prefixed with "edu.byu.ece.rapidSmith"
- GUIs built with Qt (qt jambi)
- Several javadocs and lots of documentation
- Tools for comparing XDL designs
- Excellent hard macro support (modules and module instances)



More Features Soon!

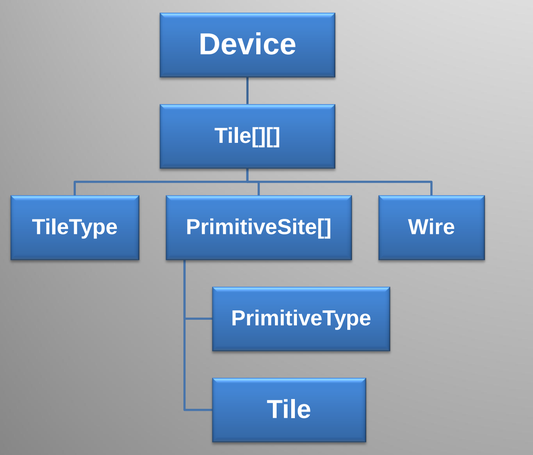
PACKAGES
- **`device`** – see box on right
- **`design`** – see box below
- **`util`** – several utilities to manipulate, analyze XDL designs in RapidSmith as well APIs to run Xilinx tools
- **`placer`** – example placers and algorithms for placing
- **`router`** – example routers and framework for building routers
- **`primitiveDefs`** – definitions of primitives found on the FPGAs
- **`examples`** – examples illustrating the capabilities of RapidSmith

RapidSmith Device Package



Screenshots of the RapidSmith Device Browser, showing primitive sites, wires and tile layouts

RAPIDSMITH DEVICES
- During installation, RapidSmith parses the large XDLRC files to generate small, fast loading device file representations
- These device files (see table below) are loaded automatically with a design
- Support up to the largest Virtex 6 parts
- RapidSmith comes with graphical viewer to browse devices (see left)



RapidSmith Device Class Hierarchy

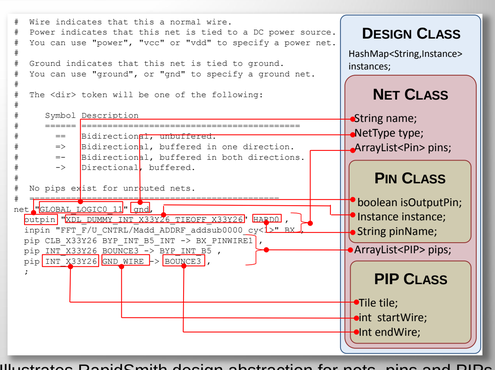
Performance of RapidSmith Device Files

Part	XDLRC Report Size	RapidSmith File Size	Java Heap Usage*	Load Time in RapidSmith*
Virtex 4 LX15	0.7 GB	232 KB	39 MB	0.48 secs
Virtex 4 FX140	7.8 GB	1546 KB	140 MB	1.63 secs
Virtex 4 LX200	9.7 GB	1011 KB	116 MB	1.53 secs
Virtex 5 LX20T	0.9 GB	497 KB	39 MB	0.52 secs
Virtex 5 FX200T	9.2 GB	1227 KB	129 MB	1.62 secs
Virtex 5 LX330T	13 GB	1250 KB	153 MB	1.91 secs
Virtex 6 LX75T	3.0 GB	583 KB	54 MB	0.79 secs
Virtex 6 HX565T	18 GB	1659 KB	125 MB	1.81 secs
Virtex 6 LX760	23 GB	1756 KB	135 MB	2.48 secs

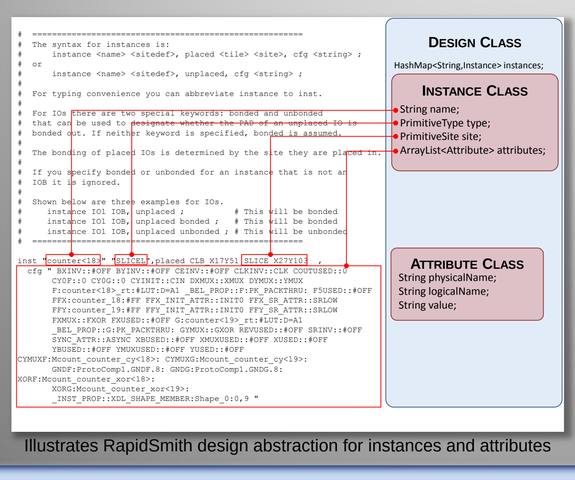
*Times and statistics were recorded on an HP workstation with an Intel Core 2 Duo 3.0 GHz processor (E6850), 4GB RAM, 500 GB SATA hard drive, Windows XP Pro SP3 32-bit and using the Oracle (previously Sun) JVM version 1.6.0_21-b07.

RapidSmith Design Package

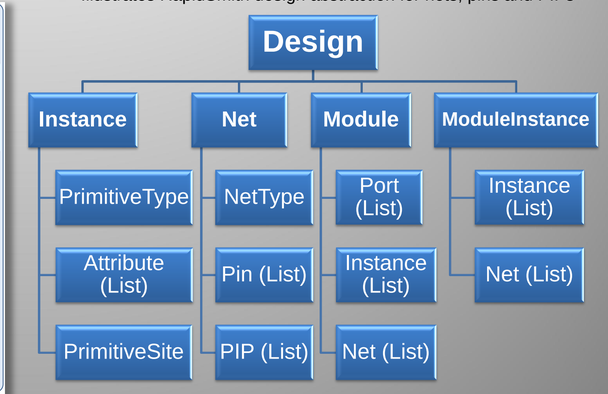
RAPIDSMITH DESIGNS
- RapidSmith designs are patterned after XDL designs
- Tile, primitive sites and wires all reference objects loaded from `Device` class
- Contains a deterministic XDL export (save) method to allow XDL "diff" easier
- Custom XDL parser to ensure speed and XDL compatibility



Illustrates RapidSmith design abstraction for nets, pins and PIPs



Illustrates RapidSmith design abstraction for instances and attributes

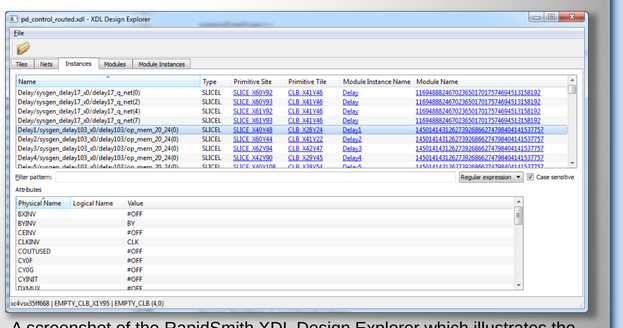


RapidSmith Design Class Hierarchy

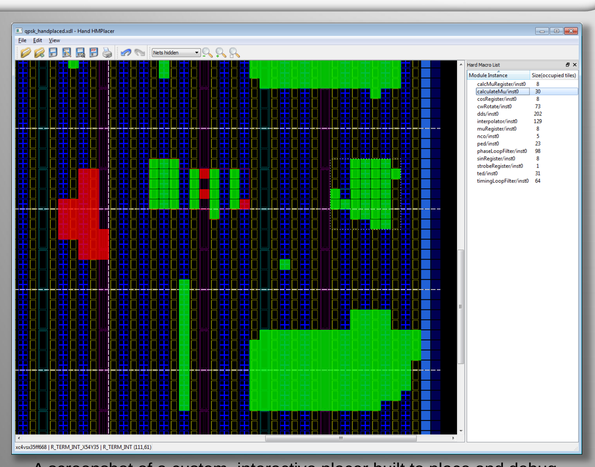
What can you do with RapidSmith?

BUILD CUSTOM TOOLS
- RapidSmith allows for rapid prototyping of custom tools and unique CAD algorithms
- Create new kinds placers, router, mappers, packers, …

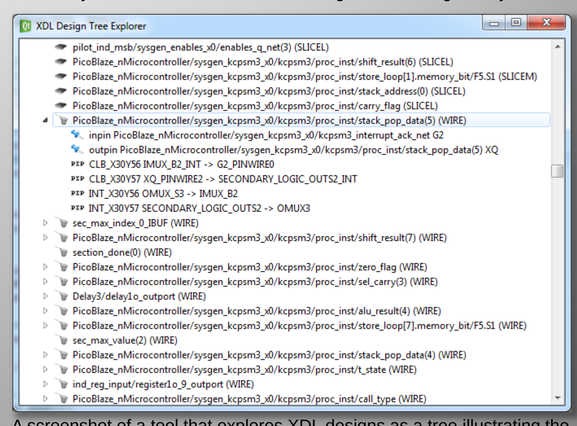
PERFORM UNIQUE DESIGN ANALYSIS
- RapidSmith provides several APIs to get at low level parts of design to extract unique design information



A screenshot of the RapidSmith XDL Design Explorer which illustrates the flexibility researchers have in constructing custom design analysis tools



A screenshot of a custom, interactive placer built to place and debug automatic hard macro placement algorithms



A screenshot of a tool that explores XDL designs as a tree illustrating the ease by which interactive design tools can be constructed in RapidSmith