

RAPIDSMITH -

RAPID PROTOTYPING FPGA DESIGN TOOLS



Christopher Lavin, Marc Padilla, Jaren Lamprecht, Philip Lundrigan, Brent Nelson, Brad Hutchings, and Michael Wirthlin

What is RapidSmith?

SUMMARY

- RapidSmith is a research-based FPGA CAD tool written in Java for modern Xilinx FPGAs
- Based on XDL, its objective is to serve as a rapid prototyping platform for research ideas and algorithms relating to low level FPGA CAD tools

DEVICE AND TOOL SUPPORT

- Currently RapidSmith supports the Xilinx FPGAs in the Virtex 4, Virtex 5 and Virtex 6 families
- It aims to be fully compatible with all modern Xilinx FPGAs
- RapidSmith works with Xilinx ISE 11.1 and above



What is XDL?

SUMMARY

- Xilinx has a human-readable native netlist equivalent to NCD called XDL
- This provides RapidSmith a gateway to create tools and manipulate Xilinx designs at a very low level

XDL DEVICE REPORTS (XDLRC FILES)

- Describes an entire FPGA and its resources •
- Represents device as a 2D array of "Tiles" ۲
 - Each tile has primitive sites, wires and PIPs
 - Enough information to build entire tool chains
- These files are very large (several gigabytes)

XDL DESIGNS

- XDL describes designs at the FPGA primitive level (SLICES, DSP, ...)
- XDL can represent designs that are:
 - unplaced and unrouted
 - partially or fully placed and unrouted
- fully placed and partially or fully routed
- XDL design files have 2 common statements:
 - instance
 - An FPGA primitive instance in the design with configuration and placement information

• net

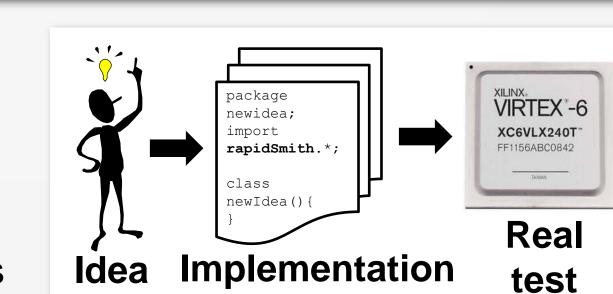
 Details pins, sources and sinks and how they are connecting in the routing resources

How RapidSmith interacts with conventional Xilinx Flow

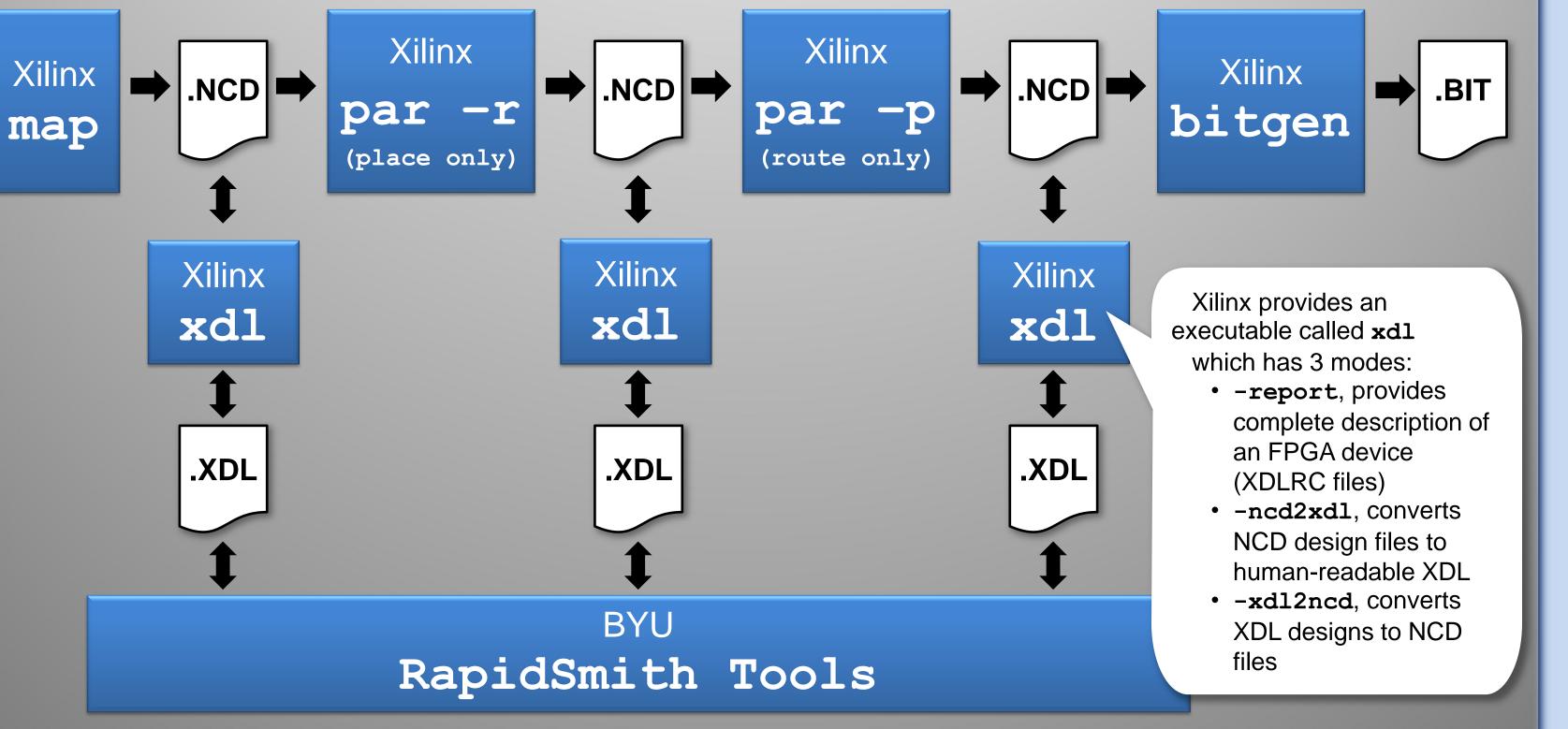


GOALS

- To provide an easy-to-use rapid prototyping platform for new FPGA CAD algorithms and ideas
- Provide useful infrastructure to demonstrate new and unique ideas on real Xilinx FPGAs







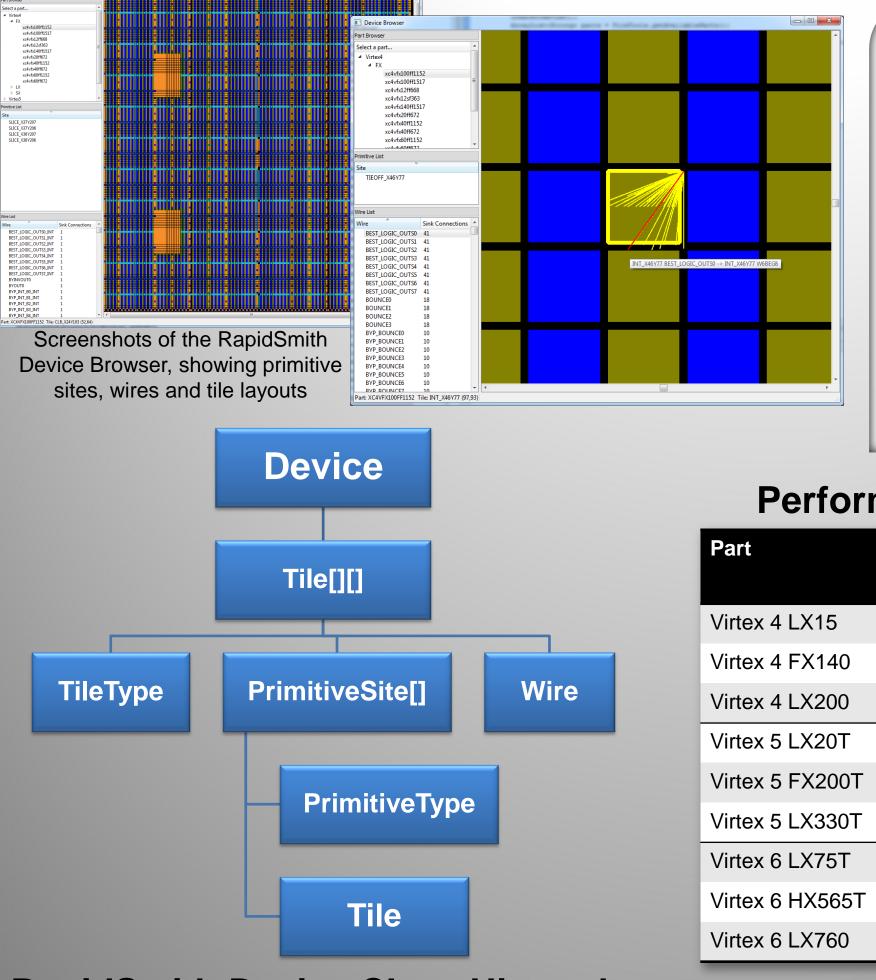
What's in RapidSmith?

OVERVIEW

- 70+ classes, over 650 APIs in RapidSmith
- 225 APIs in the design package alone for manipulating designs in RapidSmith
- Package names prefixed with "edu.byu.ece.rapidSmith" • GUIs built with Qt (qt jambi) Several javadocs and lots of documentation • Tools for comparing XDL designs • Excellent hard macro support (modules and module instances)

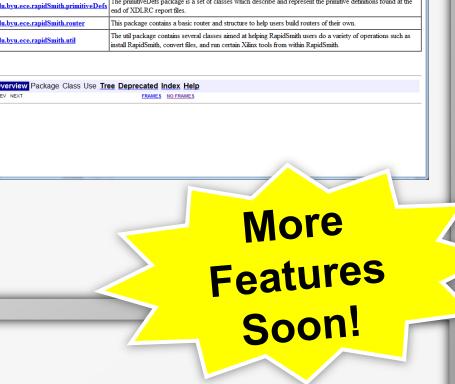
ন্দ্র ২					
ackage.					
lles, primitive sites					
ef edu.byu.ece.rapidSmith.device.helper ackage is a set of classes which are used for creating and populating the Device class and other classes in the device package.					
nection determined and the examples are the examples are the examples are the examples are the examples to illustrate how to use RapidSmith.					

RapidSmith Device Package



RAPIDSMITH DEVICES

- During installation, RapidSmith parses the large XDLRC files to generate small, fast loading device file representations



PACKAGES



device – see box on right

- design see box below
- util several utilities to manipulate, analyze XDL designs in RapidSmith as well APIs to run Xilinx tools
- placer example placers and algorithms for placing
- **router** example routers and framework for building routers
- primitiveDefs definitions of primitives found on the FPGAs
- **examples** examples illustrating the capabilities of RapidSmith

• These device files (see table below) are loaded automatically with a design

- Support up to the largest Virtex 6 parts
- RapidSmith comes with graphical viewer to browse devices (see left)

Performance of RapidSmith Device Files

Part	XDLRC Report Size	RapidSmith File Size	Java Heap Usage*	Load Time in RapidSmith*
Virtex 4 LX15	0.7 GB	232 KB	39 MB	0.48 secs
Virtex 4 FX140	7.8 GB	1546 KB	140 MB	1.63 secs
Virtex 4 LX200	9.7 GB	1011 KB	116 MB	1.53 secs
Virtex 5 LX20T	0.9 GB	497 KB	39 MB	0.52 secs
Virtex 5 FX200T	9.2 GB	1227 KB	129 MB	1.62 secs
Virtex 5 LX330T	13 GB	1250 KB	153 MB	1.91 secs
Virtex 6 LX75T	3.0 GB	583 KB	54 MB	0.79 secs
Virtex 6 HX565T	18 GB	1659 KB	125 MB	1.81 secs
Virtex 6 LX760	23 GB	1756 KB	135 MB	2.48 secs

RapidSmith Device Class Hierarchy

500 GB SATA hard drive, Windows XP Pro SP3 32-bit and using the Oracle (previously Sun) JVM version 1.6.0 21-b07

RapidSmith Design Package

RAPIDSMITH DESIGNS

- RapidSmith designs are patterned after XDL designs
- Tile, primitive sites and wires all reference objects loaded from Device class Contains a deterministic XDL export (save) method to allow XDL "diff" easier Custom XDL parser to ensure speed and XDL compatibility

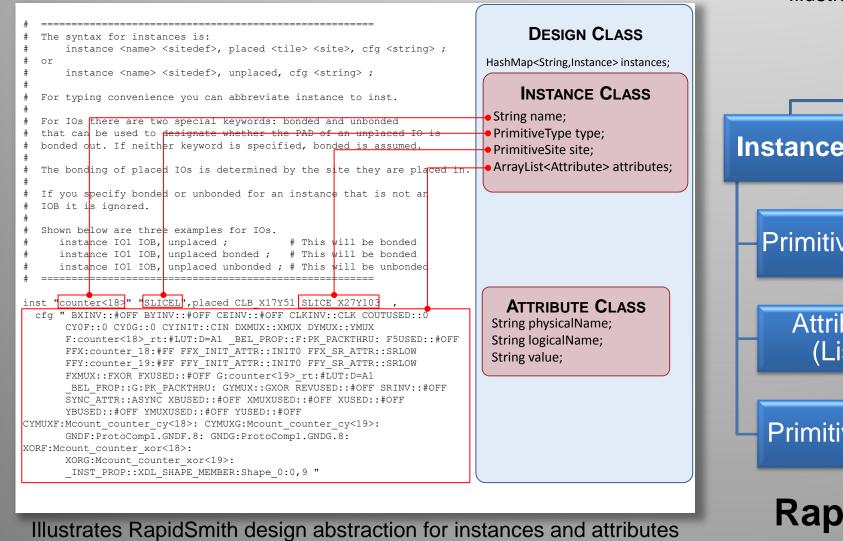
# # #	Power ind	cates that this a normal wire. icates that this net is tied to a DC power sour se "power", "vcc" or "vdd" to specify a power n	
# # #		dicates that this net is tied to ground. se "ground", or "gnd" to specify a ground net.	HashMap <string,instance> instances;</string,instance>
# # #	The <dir></dir>	token will be one of the following:	NET CLASS
#	Symbol	Description	String name;
#			-
#	==	Bidirection <mark>al, unbuffered.</mark>	NetType type;
#	=>	Bidirectional, buffered in one direction.	ArrayList <pin> pins;</pin>
#	=-	Bidirectional, buffered in both directions.	
# #	->	Directional, buffered.	
	Ma advance	xist for unrouted nets.	

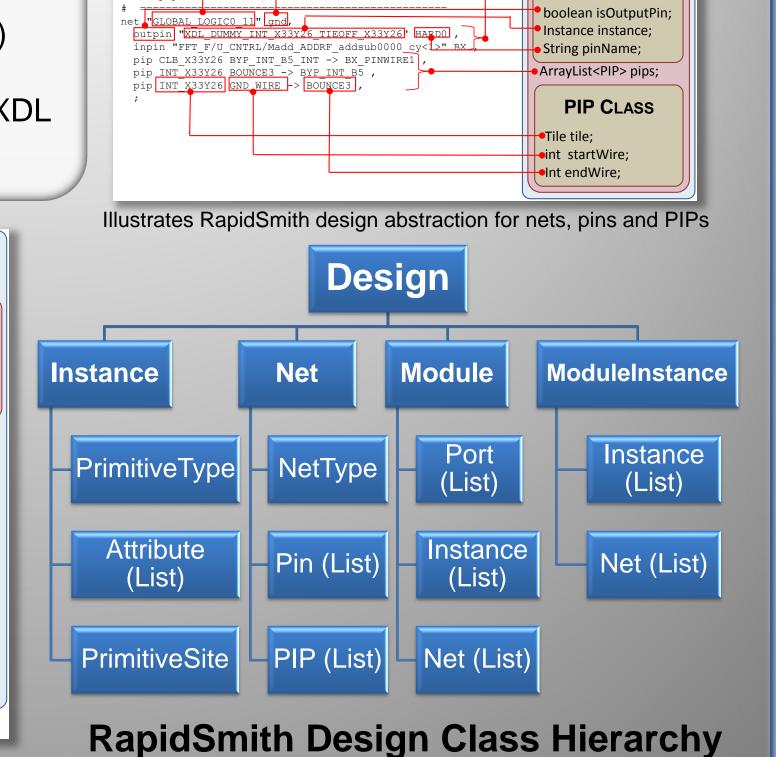
What can you do with RapidSmith?

BUILD CUSTOM TOOLS

- RapidSmith allows for rapid prototyping of custom tools and unique CAD algorithms
- Create new kinds placers, router, mappers, packers, ...

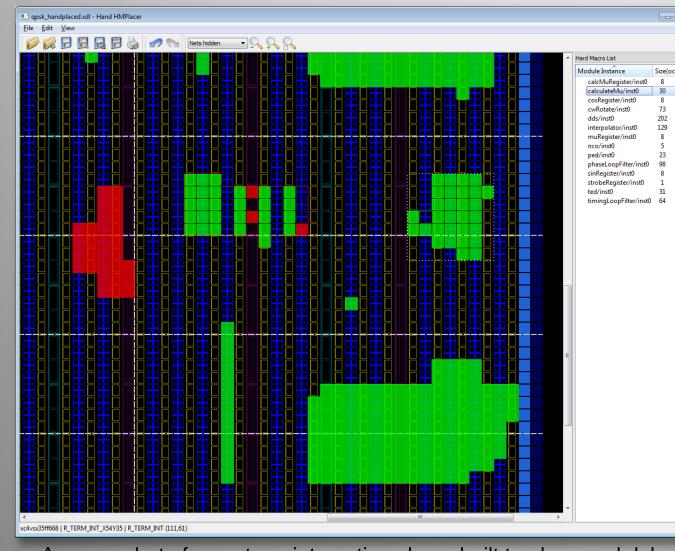
<u>F</u> ile					
<i>6</i>					
Tiles Nets Instances Modules Module Instances]				
Name	Туре	Primitive Site	Primitive Tile	Module Instance Name	Module Name
Delay/sysgen_delay17_x0/delay17_q_net(0)	SLICEL	SLICE X60Y92	CLB X41Y46	Delay	11694888246702365017017574694513158192
Delay/sysgen_delay17_x0/delay17_q_net(2)	SLICEL	SLICE X60Y93	CLB X41Y46	Delay	11694888246702365017017574694513158192
Delay/sysgen_delay17_x0/delay17_q_net(4)	SLICEL	SLICE X61Y92	CLB X41Y46	Delay	11694888246702365017017574694513158192
Delay/sysgen_delay17_x0/delay17_q_net(7)	SLICEL	SLICE X61Y93	CLB X41Y46	Delay	11694888246702365017017574694513158192
Delay1/sysgen_delay103_x0/delay103/op_mem_20_24(0)	SLICEL	SLICE X40Y48	CLB X28Y24	<u>Delay1</u>	145014143126273926866274798404141537757
Delay2/sysgen_delay103_x0/delay103/op_mem_20_24(0)	SLICEL	SLICE X60Y44	CLB X41Y22	<u>Delay2</u>	145014143126273926866274798404141537757
Delay3/sysgen_delay103_x0/delay103/op_mem_20_24(0)	SLICEL	SLICE X62Y94	CLB X42Y47	<u>Delay3</u>	145014143126273926866274798404141537757
Delay4/sysgen_delay103_x0/delay103/op_mem_20_24(0)	SLICEL	SLICE X42Y90	CLB X29Y45	<u>Delay4</u>	145014143126273926866274798404141537757
Delay5/system_delay103_v0/delay103/on_mem_20_24(0)	SLICE	SLICE VIOVIOR	CLR X28V54	Delay5	1/1501/11/1212627202686627//708//0/1/11527757





PERFORM UNIQUE DESIGN ANALYSIS

RapidSmith provides several APIs to get at low level parts of design to extract unique design information



A screenshot of a custom, interactive placer built to place and debug automatic hard macro placement algorithms

#OFF	=
BY	
#OFF	
V CLK	
JSED #OFF	
#OFF	
#OFF	
#OFF	
X #OFF	T
f668 EMPTY_CLB_X1Y95 EMPTY_CLB (4,0)	

A screenshot of the RapidSmith XDL Design Explorer which illustrates the flexibility researchers have in constructing custom design analysis tools

	pilot_ind_msb/sysgen_enables_x0/enables_q_net(3) (SLICEL)
	PicoBlaze_nMicrocontroller/sysgen_kcpsm3_x0/kcpsm3/proc_inst/shift_result(6) (SLICEL)
	PicoBlaze_nMicrocontroller/sysgen_kcpsm3_x0/kcpsm3/proc_inst/store_loop[1].memory_bit/F5.S1 (SLICEM)
	PicoBlaze_nMicrocontroller/sysgen_kcpsm3_x0/kcpsm3/proc_inst/stack_address(0) (SLICEL)
	PicoBlaze_nMicrocontroller/sysgen_kcpsm3_x0/kcpsm3/proc_inst/carry_flag (SLICEL)
_ ⊿ [PicoBlaze_nMicrocontroller/sysgen_kcpsm3_x0/kcpsm3/proc_inst/stack_pop_data(5) (WIRE)
	ኊ inpin PicoBlaze_nMicrocontroller/sysgen_kcpsm3_x0/kcpsm3_interrupt_ack_net G2
	% outpin PicoBlaze_nMicrocontroller/sysgen_kcpsm3_x0/kcpsm3/proc_inst/stack_pop_data(5) XQ
	PIP CLB_X30Y56 IMUX_B2_INT -> G2_PINWIRE0
	PIP CLB_X30Y57 XQ_PINWIRE2 -> SECONDARY_LOGIC_OUTS2_INT
	PIP INT_X30Y56 OMUX_S3 -> IMUX_B2
	PIP INT_X30Y57 SECONDARY_LOGIC_OUTS2 -> OMUX3
\triangleright	🗑 sec_max_index_0_IBUF (WIRE)
\triangleright	PicoBlaze_nMicrocontroller/sysgen_kcpsm3_x0/kcpsm3/proc_inst/shift_result(7) (WIRE)
	🗑 section_done(0) (WIRE)
\triangleright	PicoBlaze_nMicrocontroller/sysgen_kcpsm3_x0/kcpsm3/proc_inst/zero_flag (WIRE)
\triangleright	PicoBlaze_nMicrocontroller/sysgen_kcpsm3_x0/kcpsm3/proc_inst/sel_carry(3) (WIRE)
\triangleright	🗑 Delay3/delay1o_outport (WIRE)
\triangleright	PicoBlaze_nMicrocontroller/sysgen_kcpsm3_x0/kcpsm3/proc_inst/alu_result(4) (WIRE)
\triangleright	PicoBlaze_nMicrocontroller/sysgen_kcpsm3_x0/kcpsm3/proc_inst/store_loop[7].memory_bit/F5.S1 (WIRE)
	🗑 sec_max_value(2) (WIRE)
\triangleright	PicoBlaze_nMicrocontroller/sysgen_kcpsm3_x0/kcpsm3/proc_inst/stack_pop_data(4) (WIRE)
\triangleright	PicoBlaze_nMicrocontroller/sysgen_kcpsm3_x0/kcpsm3/proc_inst/t_state (WIRE)
\triangleright	🗑 ind_reg_input/register1o_9_outport (WIRE)
\triangleright	PicoBlaze_nMicrocontroller/sysgen_kcpsm3_x0/kcpsm3/proc_inst/call_type (WIRE)

ease by which interactive design tools can be constructed in RapidSmith